Remarks

Thorough examination by the Examiner is noted and appreciated.

The Specification has been amended to correct remaining grammatical errors.

The claims have been amended to clarify Applicants invention and define over the prior art.

No new matter has been added.

Support for the amendments is found in the previously presented claims as well as in the Specification at paragraph 0031:

"For example, it has been found that without a buffer layer, according to prior art processes, that ion implants to adjust a Voltage threshold shift (V_{th}) are insufficient to recover a desired Voltage threshold (V_{th}) following formation of interfacial chemical bonds at a high-K dielectric layer/gate electrode interface. As a result, formation of a buffer layer according to embodiments of the present invention improves device performance by providing more stable Voltage thresholds

and avoiding excessive Voltage threshold shifts in MOSFET device operation. **In addition, the buffer layer has the added advantage of preventing interdiffusion of metals, e.g., Si and high-K dielectric gate metals across a gate electrode/ high-K dielectric gate interface,** further improving device performance reliability. In addition, the buffer layer advantageously reduces oxygen diffusion through the high-K dielectric gate to the interfacial oxide to avoid lowering a dielectric constant, thereby avoiding device performance degradation."

Claim Rejections under 35 USC 102/103

1. Claims 22-29, 31-35, and 39-42 stand rejected under 35 USC 102(e) as anticipated, or in the alternative, under 35 USC 103(a) as being obvious over Li (2005/0202659) or Chen (2005/0269651).

Applicants note that Chen is an improperly cited reference as it has a filing date of 5/25/2005 while Applicants filing date is 3/26/2004. Applicants do no further address Chen.

Li discloses a semiconductor device (MOSFET) with **an ion implanted high-K dielectric** to reduce impurity diffusion, increase crystallization temperature, and improve thermal

stability of the high-K dielectric (paragraph 0029). **An optional buffer layer** 58 may (Figure 6b; paragraph 0046) or may not be (Figure 6a; paragraph 0045) formed on the high-K dielectric prior to ion implantation (paragraph 0030). Li teaches that the buffer layer may be made of **several types of nitrides including SiN** as well as metal silicides by polysilicon silicidation (paragraph 0030). Li teach that the buffer layer is beneficial to confine the implanted species to the high-K dielectric layer and that it may also act as a reservoir for the ion implanted species **that can diffuse into the high-K dielectric layer** (paragraphs 0030; 0047) in a subsequent annealing process. **Li teaches that if the buffer dielectric is TiN that both Ti and N may diffuse into the high-K dielectric to improve the high-K dielectric.** The buffer layer and the high-K dielectric are annealed following the implantation (paragraph 0046).

Li et al. show measurements comparing an HfON (ion implanted) to an HfO_2 High-K device showing an improvement in stability of Vt versus changing gate Voltage (paragraph 0056),

improved electron and hole mobility (paragraph 0057), reduced leakage current (paragraph 0058), improvement in subthreshold slope for a PMOS device (paragraph 0059), and improvement in time dependent dielectric breakdown (paragraph 0060).

Thus, the teachings of Li do not produce Applicants disclosed and claimed invention, but rather teach the use of a buffer layer that defeats the purpose and operation of Applicants disclosed and claimed invention and therefore is insufficient to make out a *prima facie* case of anticipation or obviousness.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki*

Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

With respect to claims 34 and 35, Applicants reject Examiners assertion of official notice "regarding the conventional recitation/use of such materials" and further note that the purpose of the recited ion implanted dopants of Li is for a completely different purpose and effect (operates by a different principal of operation) than Applicants disclosed and claimed invention.

With respect to claims 39 and 40, Applicants reject Examiners assertion of official notice "regarding the

conventional recitation/use of such materials" and further note that the recited high-K dielectrics all contain metals which may diffuse materials across a high-K dielectric interface and/or bond with gate electrode materials, a problem which Applicants invention solves and which problem is present in some of the embodiments of Li.

2. Claim 30 stands rejected under 35 USC 103(a) as being unpatentable over Li or Chen, above, and further in view of Adetutu (2005/0085092).

Applicants reiterate the comments made above with respect to Li and Chen.

Adetutu teaches forming a first dielectric layer on a semiconductor, introducing a diffusion barrier material into the first dielectric layer where the concentration of the diffusion barrier material (e.g., N) is at an upper portion of the layer, and then forming a high-K dielectric layer on the first dielectric layer. Adetutu teaches that the high concentration of

the barrier diffusion material at the interface with the overlying high-K material prevents penetration of dopants across the high-K interface (Abstract; paragraphs 0012, 0013).

Thus, modifying the buffer layer of Li to prevent dopant diffusion across the high-K dielectric interface (where Li teaches the benefits of such diffusion) would change the principal of operation of the buffer layer of Li and make it unsuitable for its intended purpose.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references

are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

3. Claims 36-38 stand rejected under 35 USC 103(a) as being unpatentable over Li or Chen, above, and further in view of Kim et al. (6,727,130) or Xiang (6,734,527).

Applicants reiterate the comments made above with respect to Li and Chen.

Even assuming *arguendo*, a proper motivation for combining the teachings of Li and Kim et al., the fact that Kim et al. teach that Al2O3, HfSiO2 **can be employed in a gate insulating (dielectric) layer**, as Examiner alleges, also does not further

help Examiner in producing Applicants disclosed and claimed structure, thus failing to make out a *prima facie* case of obviousness.

Even assuming *arguendo*, a proper motivation for combining the teachings of Li and Xaing, the fact that Xaing teaches "CMOS devices including gate materials such as hafnium silicates, aluminum oxide and their application in MOS devices including NMOS and PMOS devices, as Examiner alleges, also does not further help Examiner in producing Applicants disclosed and claimed structure, thus failing to make out a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach **or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

4. Claims 22-24, 27-29, 31-32, 34, 35, 36, 39, 40, and 42 stand rejected under 35 USC 102(e) as anticipated, or in the alternative, under 35 USC 103(a) as being obvious over Bojarczuk (2002/0190302).

Bojarczuk teaches a diffusion/reaction barrier alternatively on top of, underneath, or within a high-K dielectric layer (paragraphs 0017, 0018; 0043) to prevent reaction between the gate electrode and high-K layer and to prevent diffusion of materials from the gate electrode into the high-K dielectric (paragraph 0029). Bojarczuk teaches that in the case the diffusion/barrier layer is deposited on top of the high-K dielectric, the diffusion barrier may be **nitride or oxynitride compounds such as AlN, AlON, SiN, SiON or SiN (oxynitride)** (paragraph 0038; claim 2). Bojarczuk also teaches in this embodiment that the high-K dielectric is **formed on the semiconductor substrate** (paragraph 0032).

Bojarczuk, therefore, fails to teach the elements of Applicants invention including Applicants further claimed

dopants in the buffer dielectric layer, thus failing to anticipate or make obvious Applicants claims.

With respect to claims 31, 32, 34, 35, 39, and 40, Examiner is mistaken in equating the buffer dielectric layer AlN or AlON as having a metal dopant of Al. Bojarczuk nowhere discloses or suggests additional metal dopant (other than the components of the dielectric layer) in the buffer dielectric layer, i.e. a buffer dielectric layer could not be formed of N or ON.

Applicants reject Examiners assertion of official notice "regarding the conventional recitation/use of such materials" and again note that nowhere does Bojarczuk disclose or suggest an oxygen containing buffer dielectric further comprising a metal dopant.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051,

1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

"Finally, the prior art reference (or references when combined) must teach **or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

5. Claims 25, 26, and 41 stand rejected under 35 USC 103(a) as being unpatentable over Bojarczuk, above, and further in view of Green (2005/0042846).

Applicants reiterate the comments made above with respect to Bojarczuk.

Applicants further note that Green is an improperly applied reference since it has a filing date of 9/23/2004, post-dating the filing date of Applicants instant application. Green is therefore not further addressed.

Applicants further reject Examiners assertion of official notice "regarding the use of such conventional alternative materials for the interfacial layer" and again note that nowhere does Bojarczuk disclose or suggest an interfacial layer, but rather suggests the diffusion barrier layer underneath the high-K dielectric on the semiconductor substrate alternatively to being disposed on the high-K dielectric.

"Finally, the prior art reference (or references when combined) must teach **or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

6. Claim 30 stands rejected under 35 USC 103(a) as being unpatentable over Bojarczuk, above, and further in view of Adetutu, above.

Applicants reiterate the comments made above with respect to Bojarczuk.

Adetutu teaches forming a first dielectric layer on a semiconductor, introducing a diffusion barrier material into the first dielectric layer where the concentration of the diffusion barrier material (e.g., N) is at an upper portion of the layer, and then forming a high-K dielectric layer on the first dielectric layer. Adetutu teaches that the high concentration of the barrier diffusion material at the interface with the overlying high-K material prevents penetration of dopants across the high-K interface (Abstract; paragraphs 0012, 0013).

Thus, even assuming arguendo, a proper motivation for combining the teachings of Adetutu with Bojarczuk, the

modification of Bojarczuk (introducing a diffusion barrier material into the first dielectric layer) does not produce a buffer dielectric layer on the high-K dielectric, but only modifies the diffusion barrier material underneath the dielectric (which is an alternative embodiment to being on the high-K dielectric of Bojarczuk) and nevertheless, such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach **or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

7. Claims 31-35 stand rejected under 35 USC 103(a) as being unpatentable over Bojarczuk, above, and further in view of Paton (6,703,277) and Chen, above.

Applicants reiterate the comments made above with respect

to Bojarczuk and Chen, and therefore Chen is not further addressed since it is an improperly applied reference.

Even assuming *arguendo*, a proper motivation for combination, the fact that Paton teaches deposition a metal layer on a high-K dielectric and diffusing the metal through the high-K dielectric to an underlying oxide interfacial layer that reduces silicon dioxide to silicon and where the metal is then oxidized to form a dielectric material (interfacial layer) having a higher dielectric constant than silicon dioxide, does not further help Examiner in producing Applicants disclosed and claimed invention, and further would make the diffusion barrier layer of Bojarczuk (underneath the high-K dielectric layer) unsuitable for its intended purpose.

Applicants further reject Examiners assertion of official notice "regarding the alternative of various metal dopants" and "the conventional recitation/use of such materials" and again note that nowhere does Bojarczuk disclose or suggest metal dopants in the nitride or oxynitride layers other than the metal

component forming the metal nitride or metal oxynitride layers (AlN or AlON).

"Finally, the prior art reference (or references when combined) must teach **or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

8. Claims 36-38 stand rejected under 35 USC 103(a) as being unpatentable over Bojarczuk, above, and further in view of Kim and Xian, above.

Applicants reiterate the comments made above with respect to Bojarczuk.

Even assuming *arguendo*, a proper motivation for combining the teachings of Bojarczuk and Kim et al., the fact that Kim et al. teach that Al2O3, HfO2 **is employed in a gate insulating (dielectric) layer**, does not further help Examiner in producing

Applicants disclosed and claimed structure, thus failing to make out a *prima facie* case of obviousness.

Even assuming *arguendo*, a proper motivation for combining the teachings of Bojarczuk and Xaing, the fact that Xaing teaches "CMOS devices including gate materials such as hafnium silicates, aluminum oxide and their application in MOS devices including NMOS and PMOS devices, also does not further help Examiner in producing Applicants disclosed and claimed structure, thus failing to make out a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach **or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

The multiplicity of cited references fail to produce Applicants disclosed and claimed invention and therefore fail to make out a *prima facie* case of anticipation or obviousness with respect to Applicants independent and dependent claims.

The Claims have been further amended to further distinguish over the applied art.

Based on the foregoing, Applicants respectfully submit that the Claims are in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

U.S.S.N. 10/809,974

Respectfully submitted,

Tung & Associates

Randy W. Tung
Reg. No. 31,311
Telephone: (248) 540-4040